ABSTRACT

Described is a system and method for centralized synchronization for the transportation of data between devices in different clock domains. In a preferred embodiment, synchronization logic synchronizes read data from an asynchronous peripheral to a bus clock. Rather than being located on each peripheral, the synchronization logic is located in the bus interface logic. When there is an indication that synchronization is needed for a peripheral, the synchronization logic samples the data bus twice or more and compares the values of consecutive data samples. If the data samples are equal, this data is returned to the bus master. If they are different, the data in the next cycle is returned to the bus master.